

EAST Search History

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|-------|-------|--|---|------------------|---------|------------------|
| L3 | 30926 | (crystal\$4 crystallographic surface) adj orientation\$1 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2006/04/15 14:27 |
| L11 | 3514 | 3 and (CMOS (complementary adj metal adj oxide adj semiconductor) MOSFET\$1) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2006/04/15 15:31 |
| L12 | 584 | 11 and (epitaxial\$2 with (orientation\$1 direction\$1)) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2006/04/15 15:32 |
| L13 | 165 | 12 and (SOI (silicon adj on adj insulator)) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2006/04/15 15:32 |

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| L15 | 9838 | (SOI (silicon adj on adj insulator)) | US-PGPUB | OR | OFF | 2006/04/15 16:26 |
| L16 | 6746 | (crystal\$4 crystallographic surface) adj orientation\$1 | US-PGPUB | OR | OFF | 2006/04/15 16:27 |
| L17 | 197 | 15 same 16 | US-PGPUB | OR | OFF | 2006/04/15 16:27 |
| L18 | 31 | 17 same (polish\$3 planariz\$5) | US-PGPUB | OR | OFF | 2006/04/15 16:28 |
| L19 | 9 | 18 same (bond\$3 with wafer) | US-PGPUB | OR | OFF | 2006/04/15 16:28 |
| L20 | 1 | 19.clm. | US-PGPUB | OR | OFF | 2006/04/15 16:29 |



Inventor Name Search Result

Your Search was:

Last Name = ZHU

First Name = HUILONG

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|--------------------------|-------------------------|--------|------------|--|---------------|
| 10604907 | 6924517 | 150 | 08/26/2003 | THIN CHANNEL FET WITH RECESSED SOURCE/DRAINS AND EXTENSIONS | ZHU, HUILONG |
| 10605130 | 6908850 | 150 | 09/10/2003 | STRUCTURE AND METHOD FOR SILICIDED METAL GATE TRANSISTORS | ZHU, HUILONG |
| 10605726 | 6939751 | 150 | 10/22/2003 | METHOD AND MANUFACTURE OF THIN SILICON ON INSULATOR (SOI) WITH RECESSED CHANNEL AND DEVICES MANUFACTURED THEREBY | ZHU, HUILONG |
| 10627753 | Not Issued | 41 | 07/28/2003 | Method for slowing down dopant-enhanced diffusion in substrates and devices fabricated therefrom | ZHU, HUILONG |
| 10650229 | 6914303 | 150 | 08/28/2003 | ULTRA THIN CHANNEL MOSFET | ZHU, HUILONG |
| 10695748 | Not Issued | 41 | 10/30/2003 | Structure and method to enhance both nFET and pFET performance using different kinds of stressed layers | ZHU, HUILONG |
| 10701526 | 7015082 | 150 | 11/06/2003 | HIGH MOBILITY CMOS CIRCUITS | ZHU, HUILONG |
| 10707690 | Not Issued | 30 | 01/05/2004 | STRUCTURES AND METHODS FOR MAKING STRAINED MOSFETS | ZHU, HUILONG |
| 10707840 | Not Issued | 93 | 01/16/2004 | PROTECTING SILICON GERMANIUM SIDEWALL WITH SILICON FOR STRAINED SILICON/SILICON GERMANIUM MOSFETS | ZHU, HUILONG |
| 10707841 | Not Issued | 71 | 01/16/2004 | METHOD AND STRUCTURE FOR CONTROLLING STRESS IN A TRANSISTOR CHANNEL | ZHU, HUILONG |
| 10707842 | Not Issued | 71 | 01/16/2004 | METHOD AND APPARATUS TO INCREASE STRAIN EFFECT IN A TRANSISTOR CHANNEL | ZHU, HUILONG |
| 10708378 | Not Issued | 41 | 02/27/2004 | HYBRID SOI/BULK SEMICONDUCTOR TRANSISTORS | ZHU, HUILONG |
| 10708746 | 6881635 | 150 | 03/23/2004 | STRAINED SILICON NMOS DEVICES WITH EMBEDDED SOURCE/DRAIN | ZHU, HUILONG |

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|-----------------|------------|-----|------------|--|--------------|
| <u>10709129</u> | Not Issued | 41 | 04/15/2004 | METHODS FOR MANUFACTURING A FINFET USING A CONVENTIONAL WAFER AND APPARATUS MANUFACTURED THEREFROM | ZHU, HUILONG |
| <u>10709239</u> | Not Issued | 41 | 04/23/2004 | STRUCTURES AND METHODS FOR MANUFACTURING OF DISLOCATION FREE STRESSED CHANNELS IN BULK SILICON AND SOI CMOS DEVICES BY GATE STRESS ENGINEERING WITH SiGe AND/OR Si:C | ZHU, HUILONG |
| <u>10709248</u> | Not Issued | 41 | 04/23/2004 | structure and method of manufacturing a finFet device having stacked fins | ZHU, HUILONG |
| <u>10710244</u> | Not Issued | 41 | 06/29/2004 | STRUCTURES AND METHODS FOR MANUFACTURING P-TYPE MOSFET WITH GRADED EMBEDDED SILICON-GERMANIUM SOURCE-DRAIN AND/OR EXTENSION | ZHU, HUILONG |
| <u>10710272</u> | Not Issued | 71 | 06/30/2004 | METHOD AND STRUCTURE FOR STRAINED FINFET DEVICES | ZHU, HUILONG |
| <u>10710274</u> | 6972461 | 150 | 06/30/2004 | CHANNEL MOSFET WITH STRAINED SILICON CHANNEL ON STRAINED SIGE | ZHU, HUILONG |
| <u>10710277</u> | Not Issued | 71 | 06/30/2004 | STRUCTURE AND METHOD FOR MANUFACTURING PLANAR SOI SUBSTRATE WITH MULTIPLE ORIENTATIONS | ZHU, HUILONG |
| <u>10711080</u> | 7037818 | 150 | 08/20/2004 | APPARATUS AND METHOD FOR STAIRCASE RAISED SOURCE/DRAIN STRUCTURE | ZHU, HUILONG |
| <u>10711182</u> | Not Issued | 19 | 01/01/0001 | Structure and method of making double-gated self-aligned finfet having gates of different lengths | ZHU, HUILONG |
| <u>10711200</u> | Not Issued | 25 | 09/01/2004 | MULTI-GATE DEVICE WITH HIGH K DIELECTRIC FOR CHANNEL TOP SURFACE | ZHU, HUILONG |
| <u>10711416</u> | Not Issued | 30 | 09/17/2004 | SEMICONDUCTOR DEVICE STRUCTURE WITH ACTIVE REGIONS HAVING DIFFERENT SURFACE DIRECTIONS AND METHODS | ZHU, HUILONG |
| <u>10717737</u> | Not Issued | 71 | 11/20/2003 | Dual gate finfet | ZHU, HUILONG |
| <u>10859736</u> | Not Issued | 41 | 06/03/2004 | Strained Si on multiple materials for bulk or SOI substrates | ZHU, HUILONG |
| <u>10904059</u> | Not Issued | 51 | 10/21/2004 | CONTACT FOR DUAL LINER PRODUCT | ZHU, HUILONG |
| <u>10904460</u> | Not Issued | 61 | 11/11/2004 | Circuit and Method of Controlling Integrated Circuit Power Consumption Using Phase Change Switches | ZHU, HUILONG |

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|-----------------|------------|-----|------------|---|--------------|
| <u>10904660</u> | Not Issued | 41 | 11/22/2004 | Lowered Source/Drain Transistors | ZHU, HUILONG |
| <u>10904783</u> | 7033870 | 150 | 11/29/2004 | SEMICONDUCTOR TRANSISTORS WITH REDUCED GATE-SOURCE/DRAIN CAPACITANCES | ZHU, HUILONG |
| <u>10905025</u> | Not Issued | 30 | 12/10/2004 | DEVICE HAVING ENHANCED STRESS STATE AND RELATED METHODS | ZHU, HUILONG |
| <u>10905041</u> | Not Issued | 41 | 12/13/2004 | SIDEWALL SEMICONDUCTOR TRANSISTORS | ZHU, HUILONG |
| <u>10905062</u> | Not Issued | 30 | 12/14/2004 | DUAL STRESSED SOI SUBSTRATES | ZHU, HUILONG |
| <u>10905101</u> | Not Issued | 71 | 12/15/2004 | STRUCTURE AND METHOD TO GENERATE LOCAL MECHANICAL GATE STRESS FOR MOSFET CHANNEL MOBILITY MODIFICATION | ZHU, HUILONG |
| <u>10905454</u> | Not Issued | 30 | 01/05/2005 | METHOD OF FABRICATING A FIELD EFFECT TRANSISTOR HAVING IMPROVED JUNCTIONS | ZHU, HUILONG |
| <u>10905549</u> | Not Issued | 30 | 01/10/2005 | FULLY SILICIDED FIELD EFFECT TRANSISTORS | ZHU, HUILONG |
| <u>10905586</u> | Not Issued | 30 | 01/12/2005 | TRANSISTOR STRUCTURE HAVING STRESSED REGIONS OF OPPOSITE TYPES UNDERLYING CHANNEL AND SOURCE/DRAIN REGIONS | ZHU, HUILONG |
| <u>10905629</u> | Not Issued | 41 | 01/13/2005 | SELF-FORMING METAL SILICIDE GATE FOR CMOS DEVICES | ZHU, HUILONG |
| <u>10905710</u> | Not Issued | 41 | 01/18/2005 | STRUCTURE AND METHOD TO ENHANCE STRESS IN A CHANNEL OF CMOS DEVICES USING A THIN GATE | ZHU, HUILONG |
| <u>10905978</u> | Not Issued | 30 | 01/28/2005 | STRUCTURE AND METHOD FOR MANUFACTURING PLANAR STRAINED Si/SiGe SUBSTRATE WITH MULTIPLE ORIENTATIONS AND DIFFERENT STRESS LEVELS | ZHU, HUILONG |
| <u>10906054</u> | Not Issued | 30 | 02/01/2005 | STRUCTURE AND METHOD TO INDUCE STRAIN IN A SEMICONDUCTOR DEVICE CHANNEL WITH STRESSED FILM UNDER THE GATE | ZHU, HUILONG |
| <u>10906335</u> | Not Issued | 30 | 02/15/2005 | STRUCTURE AND METHOD FOR MANUFACTURING STRAINED FINFET | ZHU, HUILONG |
| <u>10906669</u> | Not Issued | 30 | 03/01/2005 | METHOD AND STRUCTURE FOR FORMING SELF-ALIGNED, DUAL STRESS LINER FOR CMOS DEVICES | ZHU, HUILONG |
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|--------------------------|------------|----|------------|---|--------------|
| 10907464 | Not Issued | 41 | 04/01/2005 | SEMICONDUCTOR DEVICE FORMING METHOD AND STRUCTURE FOR RETARDING DOPANT-ENHANCED DIFFUSION | ZHU, HUILONG |
| 10908087 | Not Issued | 41 | 04/27/2005 | FIELD EFFECT TRANSISTORS (FETs) WITH MULTIPLE AND/OR STAIRCASE SILICIDE | ZHU, HUILONG |
| 10954838 | Not Issued | 30 | 09/30/2004 | Structure and method for manufacturing MOSFET with super-steep retrograded island | ZHU, HUILONG |
| 10978951 | Not Issued | 93 | 11/01/2004 | DUAL FUNCTION FINFET, FINMEMORY AND METHOD OF MANUFACTURE | ZHU, HUILONG |
| 11037622 | Not Issued | 30 | 01/18/2005 | Structure and method for manufacturing strained silicon directly-on-insulator substrate with hybrid crystalline orientation and different stress levels | ZHU, HUILONG |
| 11062993 | Not Issued | 71 | 02/22/2005 | Strained silicon NMOS devices with embedded source/drain | ZHU, HUILONG |
| 11083743 | Not Issued | 30 | 03/18/2005 | Ultra thin channel MOSFET | ZHU, HUILONG |

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First Name = HUILONG

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|--------------------------|------------|--------|------------|--|---------------|
| 11160676 | Not Issued | 30 | 07/05/2005 | SELF-ALIGNED DUAL STRESSED LAYERS | ZHU, HUILONG |
| 11160698 | Not Issued | 30 | 07/06/2005 | MOSFET WITH MULTIPLE FULLY SILICIDED GATE AND METHOD FOR MAKING THE SAME | ZHU, HUILONG |
| 11161062 | Not Issued | 20 | 07/21/2005 | HIGH PERFORMANCE MOSFET COMPRISING STRESSED PHASE CHANGE MATERIAL AND METHOD OF FABRICATING THE SAME | ZHU, HUILONG |
| 11161067 | Not Issued | 30 | 07/21/2005 | UNDERCUT AND RESIDUAL SPACER PREVENTION FOR DUAL STRESSED LAYERS | ZHU, HUILONG |
| 11161068 | Not Issued | 30 | 07/21/2005 | SEMICONDUCTOR DEVICE CONTAINING HIGH PERFORMANCE P-MOSFET AND/OR N-MOSFET AND METHOD OF FABRICATING THE SAME | ZHU, HUILONG |
| 11161447 | Not Issued | 30 | 08/03/2005 | STRUCTURE AND METHOD FOR REDUCING OVERLAP CAPACITANCE IN FIELD EFFECT TRANSISTORS | ZHU, HUILONG |
| 11162126 | Not Issued | 30 | 08/30/2005 | MOSFET WITH Laterally Graded Channel Region and Method for Manufacturing Same | ZHU, HUILONG |
| 11162424 | Not Issued | 30 | 09/09/2005 | MOSFET WITH HIGH ANGLE SIDEWALL GATE AND CONTACTS FOR REDUCED MILLER CAPACITANCE | ZHU, HUILONG |
| 11162478 | Not Issued | 30 | 09/12/2005 | ANTI-HALO COMPENSATION | ZHU, HUILONG |
| 11163647 | Not Issued | 20 | 10/26/2005 | STRUCTURE AND METHOD FOR MANUFACTURING HIGH PERFORMANCE AND LOW LEAKAGE FIELD EFFECT TRANSISTOR | ZHU, HUILONG |
| 11163652 | Not Issued | 20 | 10/26/2005 | SEMICONDUCTOR SUBSTRATE WITH MULTIPLE CRYSTALLOGRAPHIC ORIENTATIONS | ZHU, HUILONG |
| 11163687 | Not | 18 | 10/27/2005 | STRUCTURE AND METHOD OF | ZHU, HUILONG |

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|--------------------------|------------|----|------------|--|--------------|
| | Issued | | | FABRICATING FINFET WITH BURIED CHANNEL | |
| 11164224 | Not Issued | 30 | 11/15/2005 | METHOD AND STRUCTURE FOR ENHANCING BOTH NMOSFET AND PMOSFET PERFORMANCE WITH A STRESSED FILM | ZHU, HUILONG |
| 11164379 | Not Issued | 19 | 01/01/0001 | SIDEWALL MOSFETS WITH EMBEDDED STRAINED SOURCE/DRAIN | ZHU, HUILONG |
| 11164568 | Not Issued | 19 | 01/01/0001 | METHOD OF MANUFACTURING A SEMICONDUCTOR STRUCTURE | ZHU, HUILONG |
| 11164621 | Not Issued | 19 | 01/01/0001 | FINFET STRUCTURE WITH MULTIPLY STRESSED GATE ELECTRODE | ZHU, HUILONG |
| 11244291 | Not Issued | 30 | 10/06/2005 | High mobility CMOS circuits | ZHU, HUILONG |
| 11278910 | Not Issued | 20 | 04/06/2006 | PROTECTING SILICON GERMANIUM SIDEWALL WITH SILICON FOR STRAINED SILICON SILICON MOSFETS | ZHU, HUILONG |
| 11306707 | Not Issued | 19 | 01/01/0001 | STRUCTURE AND METHOD FOR MAKING HIGH DENSITY MOSFET CIRCUITS WITH DIFFERENT HEIGHT CONTACT LINES | ZHU, HUILONG |
| 11306713 | Not Issued | 19 | 01/01/0001 | SEMICONDUCTOR SUBSTRATE WITH MULTIPLE CRYSTALLOGRAPHIC ORIENTATIONS | ZHU, HUILONG |
| 11306748 | Not Issued | 19 | 01/01/0001 | CMOS WITH DUAL METAL GATE | ZHU, HUILONG |
| 11307295 | Not Issued | 19 | 01/01/0001 | DUAL FUNCTION FINFET STRUCTURE AND METHOD FOR FABRICATION THEREOF | ZHU, HUILONG |
| 11308410 | Not Issued | 20 | 03/22/2006 | STRUCTURE AND METHOD FOR FABRICATING RECESSED CHANNEL MOSFET WITH FANNED OUT TAPERED SURFACE RAISED SOURCE/DRAIN | ZHU, HUILONG |
| 11308487 | Not Issued | 19 | 01/01/0001 | TEST STRUCTURES AND METHOD OF DEFECT DETECTION USING VOLTAGE CONTRAST INSPECTION | ZHU, HUILONG |

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Inventor Name Search Result

Your Search was:

Last Name = DORIS

First Name = BRUCE

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|--------------------------|-------------------------|--------|------------|--|-----------------|
| 10604196 | Not Issued | 95 | 06/30/2003 | METHODS OF PLANARIZATION | DORIS, BRUCE |
| 10536483 | Not Issued | 30 | 05/24/2005 | Strained finfet cmos device structures | DORIS, BRUCE B |
| 09841531 | Not Issued | 161 | 04/24/2001 | Formation of notched gate using a multi-layer stack | DORIS, BRUCE B. |
| 09864974 | 6645867 | 150 | 05/24/2001 | STRUCTURE AND METHOD TO PRESERVE STI DURING ETCHING | DORIS, BRUCE B. |
| 09882250 | 6586289 | 150 | 06/15/2001 | ANTI-SPACER STRUCTURE FOR IMPROVED GATE ACTIVATION | DORIS, BRUCE B. |
| 09888160 | 6531365 | 150 | 06/22/2001 | ANTI-SPACER STRUCTURE FOR SELF-ALIGNED INDEPENDENT GATE IMPLANTATION | DORIS, BRUCE B. |
| 09902830 | 6512266 | 150 | 07/11/2001 | METHOD OF FABRICATING SIO2 SPACERS AND ANNEALING CAPS | DORIS, BRUCE B. |
| 09905233 | 6566210 | 150 | 07/13/2001 | METHOD OF IMPROVING GATE ACTIVATION BY EMPLOYING ATOMIC OXYGEN ENHANCED OXIDATION | DORIS, BRUCE B. |
| 09938097 | 6642147 | 150 | 08/23/2001 | METHOD OF MAKING THERMALLY STABLE PLANARIZING FILMS | DORIS, BRUCE B. |
| 10000695 | 6509221 | 150 | 11/15/2001 | METHOD FOR FORMING HIGH PERFORMANCE CMOS DEVICES WITH ELEVATED SIDEWALL SPACERS | DORIS, BRUCE B. |
| 10078779 | 6562713 | 150 | 02/19/2002 | METHOD OF PROTECTING SEMICONDUCTOR AREAS WHILE EXPOSING A GATE | DORIS, BRUCE B. |
| 10195596 | 6657244 | 150 | 06/28/2002 | STRUCTURE AND METHOD TO REDUCE SILICON SUBSTRATE CONSUMPTION AND IMPROVE GATE SHEET RESISTANCE DURING SILICIDE FORMATION | DORIS, BRUCE B. |
| 10212938 | 6803315 | 150 | 08/05/2002 | METHOD FOR BLOCKING IMPLANTS FROM THE GATE OF AN ELECTRONIC DEVICE VIA PLANARIZING FILMS | DORIS, BRUCE B. |
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|-----------------|----------------|-----|------------|---|-----------------|
| <u>10249296</u> | <u>6790733</u> | 150 | 03/28/2003 | PRESERVING TEOS HARD MASK USING COR FOR RAISED SOURCE-DRAIN INCLUDING REMOVABLE/DISPOSABLE SPACER | DORIS, BRUCE B. |
| <u>10250047</u> | <u>6887798</u> | 150 | 05/30/2003 | STI STRESS MODIFICATION BY NITROGEN PLASMA TREATMENT FOR IMPROVING PERFORMANCE IN SMALL WIDTH DEVICES | DORIS, BRUCE B. |
| <u>10250053</u> | <u>6946358</u> | 150 | 05/30/2003 | METHOD OF FABRICATING SHALLOW TRENCH ISOLATION BY ULTRA-THIN SIMOX PROCESSING | DORIS, BRUCE B. |
| <u>10250069</u> | <u>6905941</u> | 150 | 06/02/2003 | STRUCTURE AND METHOD TO FABRICATE ULTRA-THIN SI CHANNEL DEVICES | DORIS, BRUCE B. |
| <u>10250241</u> | Not Issued | 61 | 06/17/2003 | High-performance CMOS devices on hybrid crystal oriented substrates | DORIS, BRUCE B. |
| <u>10301436</u> | <u>6686637</u> | 150 | 11/21/2002 | GATE STRUCTURE WITH INDEPENDENTLY TAILORED VERTICAL DOPING PROFILE | DORIS, BRUCE B. |
| <u>10304163</u> | <u>6838695</u> | 150 | 11/25/2002 | CMOS DEVICE STRUCTURE WITH IMPROVED PFET GATE ELECTRODE | DORIS, BRUCE B. |
| <u>10314499</u> | <u>6667197</u> | 150 | 12/06/2002 | METHOD FOR DIFFERENTIAL OXIDATION RATE REDUCTION FOR N-TYPE AND P-TYPE MATERIALS | DORIS, BRUCE B. |
| <u>10318600</u> | <u>6974981</u> | 150 | 12/12/2002 | ISOLATION STRUCTURES FOR IMPOSING STRESS PATTERNS | DORIS, BRUCE B. |
| <u>10318601</u> | <u>6717216</u> | 150 | 12/12/2002 | FIELD EFFECT TRANSISTOR WITH STRESSED CHANNEL AND METHOD FOR MAKING SAME | DORIS, BRUCE B. |
| <u>10318602</u> | <u>6825529</u> | 150 | 12/12/2002 | STRESS INDUCING SPACERS | DORIS, BRUCE B. |
| <u>10328234</u> | <u>6833569</u> | 150 | 12/23/2002 | SELF-ALIGNED PLANAR DOUBLE-GATE PROCESS BY AMORPHIZATION | DORIS, BRUCE B. |
| <u>10338071</u> | <u>6764883</u> | 150 | 01/07/2003 | AMORPHOUS AND POLYCRYSTALLINE SILICON NANOLAMINATE | DORIS, BRUCE B. |
| <u>10338930</u> | <u>6780694</u> | 150 | 01/08/2003 | MOS TRANSISTOR | DORIS, BRUCE B. |
| <u>10342423</u> | <u>6806534</u> | 150 | 01/14/2003 | DAMASCENE METHOD FOR IMPROVED MOS TRANSISTOR | DORIS, BRUCE B. |
| <u>10345472</u> | <u>6841826</u> | 150 | 01/15/2003 | LOW-GIDL MOSFET STRUCTURE AND METHOD FOR FABRICATION | DORIS, BRUCE B. |
| <u>10375608</u> | Not Issued | 41 | 02/27/2003 | Anti-spacer structure for improved gate activation | DORIS, BRUCE B. |
| <u>10437370</u> | Not Issued | 161 | 05/13/2003 | Structure and method to preserve STI during etching | DORIS, BRUCE B. |
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| <u>10604097</u> | <u>6911383</u> | 150 | 06/26/2003 | HYBRID PLANAR AND FINFET CMOS DEVICES | DORIS, BRUCE B. |
| <u>10604190</u> | Not Issued | 93 | 06/30/2003 | HIGH PERFORMANCE CMOS DEVICE STRUCTURES AND METHOD OF MANUFACTURE | DORIS, BRUCE B. |
| <u>10604382</u> | <u>6812105</u> | 150 | 07/16/2003 | ULTRA-THIN CHANNEL DEVICE WITH RAISED SOURCE AND DRAIN AND SOLID SOURCE EXTENSION DOPING | DORIS, BRUCE B. |
| <u>10604907</u> | <u>6924517</u> | 150 | 08/26/2003 | THIN CHANNEL FET WITH RECESSED SOURCE/DRAINS AND EXTENSIONS | DORIS, BRUCE B. |
| <u>10605130</u> | <u>6908850</u> | 150 | 09/10/2003 | STRUCTURE AND METHOD FOR SILICIDED METAL GATE TRANSISTORS | DORIS, BRUCE B. |
| <u>10605672</u> | Not Issued | 93 | 10/16/2003 | HIGH PERFORMANCE STRAINED CMOS DEVICES | DORIS, BRUCE B. |
| <u>10605697</u> | <u>6911384</u> | 150 | 10/21/2003 | GATE STRUCTURE WITH INDEPENDENTLY TAILORED VERTICAL DOPING PROFILE | DORIS, BRUCE B. |
| <u>10605726</u> | <u>6939751</u> | 150 | 10/22/2003 | METHOD AND MANUFACTURE OF THIN SILICON ON INSULATOR (SOI) WITH RECESSED CHANNEL AND DEVICES MANUFACTURED THEREBY | DORIS, BRUCE B. |
| <u>10605727</u> | <u>6989318</u> | 150 | 10/22/2003 | METHOD FOR REDUCING SHALLOW TRENCH ISOLATION CONSUMPTION IN SEMICONDUCTOR DEVICES | DORIS, BRUCE B. |
| <u>10605889</u> | <u>6982196</u> | 150 | 11/04/2003 | OXIDATION METHOD FOR ALTERING A FILM STRUCTURE AND CMOS TRANSISTOR STRUCTURE FORMED THEREWITH | DORIS, BRUCE B. |
| <u>10650229</u> | <u>6914303</u> | 150 | 08/28/2003 | ULTRA THIN CHANNEL MOSFET | DORIS, BRUCE B. |
| <u>10663471</u> | Not Issued | 161 | 09/15/2003 | Self-aligned planar double-gate process by self-aligned oxidation | DORIS, BRUCE B. |
| <u>10669727</u> | <u>6884667</u> | 150 | 09/25/2003 | FIELD EFFECT TRANSISTOR WITH STRESSED CHANNEL AND METHOD FOR MAKING SAME | DORIS, BRUCE B. |
| <u>10695748</u> | Not Issued | 41 | 10/30/2003 | Structure and method to enhance both nFET and pFET performance using different kinds of stressed layers | DORIS, BRUCE B. |
| <u>10695752</u> | <u>6977194</u> | 150 | 10/30/2003 | STRUCTURE AND METHOD TO IMPROVE CHANNEL MOBILITY BY GATE ELECTRODE STRESS MODIFICATION | DORIS, BRUCE B. |
| <u>10701526</u> | <u>7015082</u> | 150 | 11/06/2003 | HIGH MOBILITY CMOS CIRCUITS | DORIS, BRUCE B. |
| <u>10707018</u> | Not | 41 | 11/14/2003 | STRESSED SEMICONDUCTOR DEVICE | DORIS, BRUCE B. |

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| | Issued | | | STRUCTURES HAVING GRANULAR SEMICONDUCTOR MATERIAL | |
| 10707690 | Not Issued | 30 | 01/05/2004 | STRUCTURES AND METHODS FOR MAKING STRAINED MOSFETS | DORIS, BRUCE B. |
| 10707840 | Not Issued | 93 | 01/16/2004 | PROTECTING SILICON GERMANIUM SIDEWALL WITH SILICON FOR STRAINED SILICON/SILICON GERMANIUM MOSFETS | DORIS, BRUCE B. |

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First Name = BRUCE

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|--------------------------|------------|--------|------------|--|-----------------|
| 10707878 | Not Issued | 41 | 01/20/2004 | Polycrystalline Silicon Layer With Nano-grain Structure and Method of Manufacture | DORIS, BRUCE B. |
| 10708378 | Not Issued | 41 | 02/27/2004 | HYBRID SOI/BULK SEMICONDUCTOR TRANSISTORS | DORIS, BRUCE B. |
| 10708430 | Not Issued | 95 | 03/03/2004 | MOBILITY ENHANCED CMOS DEVICES | DORIS, BRUCE B. |
| 10708451 | Not Issued | 71 | 03/04/2004 | PLANAR PEDESTAL MULTI GATE DEVICE | DORIS, BRUCE B. |
| 10709129 | Not Issued | 41 | 04/15/2004 | METHODS FOR MANUFACTURING A FINFET USING A CONVENTIONAL WAFER AND APPARATUS MANUFACTURED THEREFROM | DORIS, BRUCE B. |
| 10709239 | Not Issued | 41 | 04/23/2004 | STRUCTURES AND METHODS FOR MANUFACTURING OF DISLOCATION FREE STRESSED CHANNELS IN BULK SILICON AND SOI CMOS DEVICES BY GATE STRESS ENGINEERING WITH SiGe AND/OR Si:C | DORIS, BRUCE B. |
| 10709248 | Not Issued | 41 | 04/23/2004 | structure and method of manufacturing a finFet device having stacked fins | DORIS, BRUCE B. |
| 10709314 | 6989323 | 150 | 04/28/2004 | METHOD FOR FORMING NARROW GATE STRUCTURES ON SIDEWALLS OF A LITHOGRAPHICALLY DEFINED SACRIFICIAL MATERIAL | DORIS, BRUCE B. |
| 10710273 | Not Issued | 93 | 06/30/2004 | ULTRA THIN BODY FULLY-DEPLETED SOI MOSFETS | DORIS, BRUCE B. |
| 10710277 | Not Issued | 71 | 06/30/2004 | STRUCTURE AND METHOD FOR MANUFACTURING PLANAR SOI SUBSTRATE WITH MULTIPLE ORIENTATIONS | DORIS, BRUCE B. |
| 10711182 | Not Issued | 19 | 01/01/0001 | Structure and method of making double-gated self-aligned finfet having gates of different lengths | DORIS, BRUCE B. |
| 10711200 | Not Issued | 25 | 09/01/2004 | MULTI-GATE DEVICE WITH HIGH K DIELECTRIC FOR CHANNEL TOP SURFACE | DORIS, BRUCE B. |

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|-----------------|------------|-----|------------|---|-----------------|
| <u>10711416</u> | Not Issued | 30 | 09/17/2004 | SEMICONDUCTOR DEVICE STRUCTURE WITH ACTIVE REGIONS HAVING DIFFERENT SURFACE DIRECTIONS AND METHODS | DORIS, BRUCE B. |
| <u>10717737</u> | Not Issued | 71 | 11/20/2003 | Dual gate finfet | DORIS, BRUCE B. |
| <u>10722873</u> | Not Issued | 95 | 11/26/2003 | STRUCTURE AND METHOD TO FABRICATE FINFET DEVICES | DORIS, BRUCE B. |
| <u>10725848</u> | Not Issued | 61 | 12/02/2003 | Ultra-thin Si MOSFET device structure and method of manufacture | DORIS, BRUCE B. |
| <u>10725849</u> | Not Issued | 93 | 12/02/2003 | ULTRA-THIN SI CHANNEL MOSFET USING A SELF-ALIGNED OXYGEN IMPLANT AND DAMASCENE TECHNIQUE | DORIS, BRUCE B. |
| <u>10732322</u> | Not Issued | 61 | 12/10/2003 | Sectional field effect devices and method of fabrication | DORIS, BRUCE B. |
| <u>10735736</u> | 7018891 | 150 | 12/16/2003 | ULTRA-THIN SI CHANNEL CMOS WITH IMPROVED SERIES RESISTANCE | DORIS, BRUCE B. |
| <u>10751831</u> | Not Issued | 41 | 01/05/2004 | STI STRESS MODIFICATION BY NITROGEN PLASMA TREATMENT FOR IMPROVING PERFORMANCE IN SMALL WIDTH DEVICES | DORIS, BRUCE B. |
| <u>10793084</u> | Not Issued | 71 | 03/04/2004 | Amorphous and polycrystalline silicon nanolaminate | DORIS, BRUCE B. |
| <u>10862073</u> | Not Issued | 83 | 06/04/2004 | Structure and method to fabricate ultra-thin Si channel devices | DORIS, BRUCE B. |
| <u>10872605</u> | Not Issued | 61 | 06/21/2004 | Hybrid substrate technology for high-mobility planar and multiple-gate MOSFETs | DORIS, BRUCE B. |
| <u>10876873</u> | 6878582 | 150 | 06/25/2004 | LOW-GIDL MOSFET STRUCTURE AND METHOD FOR FABRICATION | DORIS, BRUCE B. |
| <u>10904391</u> | Not Issued | 71 | 11/08/2004 | SELF-ALIGNED LOW-k GATE CAP | DORIS, BRUCE B. |
| <u>10905062</u> | Not Issued | 30 | 12/14/2004 | DUAL STRESSED SOI SUBSTRATES | DORIS, BRUCE B. |
| <u>10905101</u> | Not Issued | 71 | 12/15/2004 | STRUCTURE AND METHOD TO GENERATE LOCAL MECHANICAL GATE STRESS FOR MOSFET CHANNEL MOBILITY MODIFICATION | DORIS, BRUCE B. |
| <u>10905477</u> | Not Issued | 71 | 01/06/2005 | METHOD OF CREATING A Ge-RICH CHANNEL LAYER FOR HIGH-PERFORMANCE CMOS CIRCUITS | DORIS, BRUCE B. |
| <u>10905978</u> | Not Issued | 30 | 01/28/2005 | STRUCTURE AND METHOD FOR MANUFACTURING PLANAR STRAINED Si/SiGe SUBSTRATE WITH MULTIPLE ORIENTATIONS AND | DORIS, BRUCE B. |

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|-----------------|------------|----|------------|---|-----------------|
| | | | | DIFFERENT STRESS LEVELS | |
| <u>10906335</u> | Not Issued | 30 | 02/15/2005 | STRUCTURE AND METHOD FOR MANUFACTURING STRAINED FINFET | DORIS, BRUCE B. |
| <u>10916814</u> | Not Issued | 61 | 08/12/2004 | Ultra-thin channel device with raised source and drain and solid source extension doping | DORIS, BRUCE B. |
| <u>10935136</u> | Not Issued | 30 | 09/07/2004 | Stress inducing spacers | DORIS, BRUCE B. |
| <u>10978951</u> | Not Issued | 93 | 11/01/2004 | DUAL FUNCTION FINFET, FINMEMORY AND METHOD OF MANUFACTURE | DORIS, BRUCE B. |
| <u>11037622</u> | Not Issued | 30 | 01/18/2005 | Structure and method for manufacturing strained silicon directly-on-insulator substrate with hybrid crystalline orientation and different stress levels | DORIS, BRUCE B. |
| <u>11083743</u> | Not Issued | 30 | 03/18/2005 | Ultra thin channel MOSFET | DORIS, BRUCE B. |
| <u>11111592</u> | Not Issued | 30 | 04/21/2005 | Using metal/metal nitride bilayers as gate electrodes in self-aligned aggressively scaled CMOS devices | DORIS, BRUCE B. |
| <u>11122193</u> | Not Issued | 30 | 05/04/2005 | Hybrid planar and FinFET CMOS devices | DORIS, BRUCE B. |
| <u>11151506</u> | Not Issued | 30 | 06/13/2005 | Structure and method to preserve STI during etching | DORIS, BRUCE B. |
| <u>11162780</u> | Not Issued | 30 | 09/22/2005 | HIGHLY MANUFACTURABLE SRAM CELLS IN SUBSTRATES WITH HYBRID CRYSTAL ORIENTATION | DORIS, BRUCE B. |
| <u>11164224</u> | Not Issued | 30 | 11/15/2005 | METHOD AND STRUCTURE FOR ENHANCING BOTH NMOSFET AND PMOSFET PERFORMANCE WITH A STRESSED FILM | DORIS, BRUCE B. |
| <u>11175223</u> | Not Issued | 30 | 07/07/2005 | Structure and method to improve channel mobility by gate electrode stress modification | DORIS, BRUCE B. |
| <u>11200958</u> | Not Issued | 20 | 08/10/2005 | Isolation structures for imposing stress patterns | DORIS, BRUCE B. |
| <u>11201163</u> | Not Issued | 30 | 08/11/2005 | Structure and method to improve channel mobility by gate electrode stress modification | DORIS, BRUCE B. |
| <u>11208360</u> | Not Issued | 30 | 08/19/2005 | Method of fabricating shallow trench isolation by ultra-thin simox processing | DORIS, BRUCE B. |
| <u>11244291</u> | Not Issued | 30 | 10/06/2005 | High mobility CMOS circuits | DORIS, BRUCE B. |
| <u>11259483</u> | Not Issued | 41 | 10/26/2005 | Structure and method to fabricate finfet devices | DORIS, BRUCE B. |
| <u>11259654</u> | Not | 30 | 10/26/2005 | Method for tuning epitaxial growth by | DORIS, BRUCE B. |

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|--------------------------|------------|----|------------|---|-----------------|
| | Issued | | | interfacial doping and structure including same | |
| 11278910 | Not Issued | 20 | 04/06/2006 | PROTECTING SILICON GERMANIUM SIDEWALL WITH SILICON FOR STRAINED SILICON SILICON MOSFETS | DORIS, BRUCE B. |
| 11303715 | Not Issued | 30 | 12/16/2005 | Dual metal gate self-aligned integration | DORIS, BRUCE B. |
| 11307671 | Not Issued | 30 | 02/16/2006 | CMOS Gate Structures Fabricated By Selective Oxidation | DORIS, BRUCE B. |

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| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|--------------------------|-------------------------|--------|------------|--|----------------------|
| 11318818 | Not Issued | 30 | 12/27/2005 | Oxidation method for altering a film structure | DORIS, BRUCE B. |
| 11318844 | Not Issued | 20 | 12/27/2005 | CMOS transistor structure including film having reduced stress by exposure to atomic oxygen | DORIS, BRUCE B. |
| 11320330 | Not Issued | 20 | 12/28/2005 | Metal gate CMOS with at least a single gate metal and dual gate dielectrics | DORIS, BRUCE B. |
| 11323564 | Not Issued | 19 | 12/30/2005 | High performance circuit with metal and polygate electrodes | DORIS, BRUCE B. |
| 11323578 | Not Issued | 19 | 12/30/2005 | High performance CMOS circuits, and methods for fabricating the same | DORIS, BRUCE B. |
| 11336727 | Not Issued | 20 | 01/20/2006 | Introduction of metal impurity to change workfunction of conductive electrodes | DORIS, BRUCE B. |
| 11362773 | Not Issued | 20 | 02/28/2006 | Mobility enhanced CMOS devices | DORIS, BRUCE B. |
| 08172974 | 5383354 | 150 | 12/27/1993 | PROCESS FOR MEASURING SURFACE TOPOGRAPHY USING ATOMIC FORCE MICROSCOPY | DORIS, BRUCE B. |
| 10015239 | 6613602 | 150 | 12/13/2001 | MONOLITHICALLY INTEGRATED COLD POINT THERMOELECTRIC COOLER | DORIS, BRUCE BENNETT |
| 10160540 | 6709926 | 150 | 05/31/2002 | HIGH PERFORMANCE LOGIC AND HIGH DENSITY EMBEDDED DRAM WITH BORDERLESS CONTACT AND ANTISPACER | DORIS, BRUCE BENNETT |
| 10682430 | 6873010 | 150 | 10/10/2003 | HIGH PERFORMANCE LOGIC AND HIGH DENSITY EMBEDDED DRAM WITH BORDERLESS CONTACT AND ANTISPACER | DORIS, BRUCE BENNETT |
| 10710272 | Not Issued | 71 | 06/30/2004 | METHOD AND STRUCTURE FOR STRAINED FINFET DEVICES | DORIS, BRUCE BENNETT |
| 11060784 | Not Issued | 93 | 02/18/2005 | HIGH PERFORMANCE STRAINED CMOS DEVICES | DORIS, BRUCE D. |

Inventor Search Completed: No Records to Display.

Last Name

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Your Search was:

Last Name = IEONG

First Name = MEIKEI

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|--------------------------|-------------------------|--------|------------|---|---------------|
| 09503926 | 6271094 | 150 | 02/14/2000 | Method of making mosfet with high dielectric constant gate insulator and minimum overlap capacitance | IEONG, MEIKEI |
| 09866239 | 6353249 | 150 | 05/25/2001 | Mosfet with high dielectric constant gate insulator and minimum overlap capacitance | IEONG, MEIKEI |
| 09886681 | Not Issued | 161 | 06/21/2001 | Mosfet having a variable gate oxide thickness and a variable gate work function, and a method for making the same | IEONG, MEIKEI |
| 09886823 | 6960806 | 150 | 06/21/2001 | DOUBLE GATED VERTICAL TRANSISTOR WITH DIFFERENT FIRST AND SECOND GATE MATERIALS | IEONG, MEIKEI |
| 09972172 | 6492212 | 150 | 10/05/2001 | VARIABLE THRESHOLD VOLTAGE DOUBLE GATED TRANSISTORS AND METHOD OF FABRICATION | IEONG, MEIKEI |
| 10117959 | 6677646 | 150 | 04/05/2002 | METHOD AND STRUCTURE OF A DISPOSABLE REVERSED SPACER PROCESS FOR HIGH PERFORMANCE RECESSED CHANNEL CMOS | IEONG, MEIKEI |
| 10127196 | 6762469 | 150 | 04/19/2002 | HIGH PERFORMANCE CMOS DEVICE STRUCTURE WITH MID-GAP METAL GATE | IEONG, MEIKEI |
| 10242941 | Not Issued | 164 | 09/13/2002 | VARIABLE THRESHOLD VOLTAGE DOUBLE GATED TRANSISTORS | IEONG, MEIKEI |
| 10250069 | 6905941 | 150 | 06/02/2003 | STRUCTURE AND METHOD TO FABRICATE ULTRA-THIN SI CHANNEL DEVICES | IEONG, MEIKEI |
| 10250241 | Not Issued | 61 | 06/17/2003 | High-performance CMOS devices on hybrid crystal oriented substrates | IEONG, MEIKEI |
| 10328234 | 6833569 | 150 | 12/23/2002 | SELF-ALIGNED PLANAR DOUBLE-GATE PROCESS BY AMORPHIZATION | IEONG, MEIKEI |
| 10328285 | 6946696 | 150 | 12/23/2002 | SELF-ALIGNED ISOLATION DOUBLE-GATE FET | IEONG, MEIKEI |
| 10604097 | 6911383 | 150 | 06/26/2003 | HYBRID PLANAR AND FINFET CMOS | IEONG, MEIKEI |

| | | | | DEVICES | |
|-----------------|----------------|-----|------------|--|---------------|
| <u>10634446</u> | <u>6830962</u> | 150 | 08/05/2003 | SELF-ALIGNED SOI WITH DIFFERENT CRYSTAL ORIENTATION USING WAFER BONDING AND SIMOX PROCESSES | IEONG, MEIKEI |
| <u>10647395</u> | <u>6815278</u> | 150 | 08/25/2003 | ULTRA-THIN SILICON-ON-INSULATOR AND STRAINED-SILICON-DIRECT-ON-INSULATOR WITH HYBRID CRYSTAL ORIENTATIONS | IEONG, MEIKEI |
| <u>10650229</u> | <u>6914303</u> | 150 | 08/28/2003 | ULTRA THIN CHANNEL MOSFET | IEONG, MEIKEI |
| <u>10663471</u> | Not Issued | 161 | 09/15/2003 | Self-aligned planar double-gate process by self-aligned oxidation | IEONG, MEIKEI |
| <u>10669898</u> | Not Issued | 93 | 09/24/2003 | METHOD AND APPARATUS FOR FABRICATING CMOS FIELD EFFECT TRANSISTORS | IEONG, MEIKEI |
| <u>10674644</u> | <u>6821826</u> | 150 | 09/30/2003 | THREE DIMENSIONAL CMOS INTEGRATED CIRCUITS HAVING DEVICE LAYERS BUILT ON DIFFERENT CRYSTAL ORIENTED WAFERS | IEONG, MEIKEI |
| <u>10696634</u> | <u>7023055</u> | 150 | 10/29/2003 | CMOS ON HYBRID SUBSTRATE WITH DIFFERENT CRYSTAL ORIENTATIONS USING SILICON-TO-SILICON DIRECT WAFER BONDING | IEONG, MEIKEI |
| <u>10710273</u> | Not Issued | 93 | 06/30/2004 | ULTRA THIN BODY FULLY-DEPLETED SOI MOSFETS | IEONG, MEIKEI |
| <u>10710277</u> | Not Issued | 71 | 06/30/2004 | STRUCTURE AND METHOD FOR MANUFACTURING PLANAR SOI SUBSTRATE WITH MULTIPLE ORIENTATIONS | IEONG, MEIKEI |
| <u>10710736</u> | <u>7002214</u> | 150 | 07/30/2004 | ULTRA-THIN BODY SUPER-STEEP RETROGRADE WELL (SSRW) FET DEVICES | IEONG, MEIKEI |
| <u>10711416</u> | Not Issued | 30 | 09/17/2004 | SEMICONDUCTOR DEVICE STRUCTURE WITH ACTIVE REGIONS HAVING DIFFERENT SURFACE DIRECTIONS AND METHODS | IEONG, MEIKEI |
| <u>10713971</u> | Not Issued | 95 | 11/14/2003 | METHOD AND STRUCTURE OF A DISPOSABLE REVERSED SPACER PROCESS FOR HIGH PERFORMANCE RECESSED CHANNEL CMOS | IEONG, MEIKEI |
| <u>10725848</u> | Not Issued | 61 | 12/02/2003 | Ultra-thin Si MOSFET device structure and method of manufacture | IEONG, MEIKEI |
| <u>10725849</u> | Not Issued | 93 | 12/02/2003 | ULTRA-THIN SI CHANNEL MOSFET USING A SELF-ALIGNED OXYGEN IMPLANT AND DAMASCENE TECHNIQUE | IEONG, MEIKEI |

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| <u>10732322</u> | Not Issued | 61 | 12/10/2003 | Sectional field effect devices and method of fabrication | IEONG, MEIKEI |
| <u>10735736</u> | <u>7018891</u> | 150 | 12/16/2003 | ULTRA-THIN SI CHANNEL CMOS WITH IMPROVED SERIES RESISTANCE | IEONG, MEIKEI |
| <u>10795672</u> | <u>6916698</u> | 150 | 03/08/2004 | HIGH PERFORMANCE CMOS DEVICE STRUCTURE WITH MID-GAP METAL GATE | IEONG, MEIKEI |
| <u>10799380</u> | <u>7023057</u> | 150 | 03/12/2004 | CMOS ON HYBRID SUBSTRATE WITH DIFFERENT CRYSTAL ORIENTATIONS USING SILICON-TO-SILICON DIRECT WAFER BONDING | IEONG, MEIKEI |
| <u>10830347</u> | Not Issued | 93 | 04/22/2004 | STRAINED SILICON CMOS ON HYBRID CRYSTAL ORIENTATIONS | IEONG, MEIKEI |
| <u>10862073</u> | Not Issued | 83 | 06/04/2004 | Structure and method to fabricate ultra-thin Si channel devices | IEONG, MEIKEI |
| <u>10872605</u> | Not Issued | 61 | 06/21/2004 | Hybrid substrate technology for high-mobility planar and multiple-gate MOSFETs | IEONG, MEIKEI |
| <u>10876155</u> | Not Issued | 71 | 06/24/2004 | Integration of strained Ge into advanced CMOS technology | IEONG, MEIKEI |
| <u>10914433</u> | Not Issued | 71 | 08/09/2004 | Three dimensional CMOS integrated circuits having device layers built on different crystal oriented wafers | IEONG, MEIKEI |
| <u>10919121</u> | Not Issued | 41 | 08/16/2004 | Three dimensional integrated circuit and method of design | IEONG, MEIKEI |
| <u>10932982</u> | Not Issued | 71 | 09/02/2004 | Ultra-thin silicon-on-insulator and strained-silicon-direct-on-insulator with hybrid crystal orientations | IEONG, MEIKEI |
| <u>10967398</u> | Not Issued | 41 | 10/18/2004 | Self-aligned SOI with different crystal orientation using WAFER bonding and SIMOX processes | IEONG, MEIKEI |
| <u>10980220</u> | Not Issued | 41 | 11/03/2004 | Enhancement of electron and hole mobilities in <110> Si under biaxial compressive strain | IEONG, MEIKEI |
| <u>10992150</u> | Not Issued | 41 | 11/18/2004 | Method to form Si-containing SOI and underlying substrate with different orientations | IEONG, MEIKEI |
| <u>11001913</u> | Not Issued | 41 | 12/02/2004 | Method and process to make multiple-threshold metal gates CMOS technology | IEONG, MEIKEI |
| <u>11029797</u> | Not Issued | 30 | 01/05/2005 | Stressed field effect transistors on hybrid orientation substrate | IEONG, MEIKEI |
| <u>11066659</u> | Not Issued | 30 | 02/25/2005 | Structure and method of fabricating a hybrid substrate for high-performance hybrid-orientation silicon-on-insulator CMOS devices | IEONG, MEIKEI |
| <u>11083743</u> | Not Issued | 30 | 03/18/2005 | Ultra thin channel MOSFET | IEONG, MEIKEI |

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| 11112820 | Not Issued | 30 | 04/22/2005 | Strained complementary metal oxide semiconductor (CMOS) on rotated wafers and methods thereof | IEONG, MEIKEI |
| 11122193 | Not Issued | 30 | 05/04/2005 | Hybrid planar and FinFET CMOS devices | IEONG, MEIKEI |
| 11125063 | Not Issued | 30 | 05/09/2005 | Double gated transistor and method of fabrication | IEONG, MEIKEI |
| 11146624 | Not Issued | 61 | 06/07/2005 | Self-aligned isolation double-gate get | IEONG, MEIKEI |
| 11160668 | Not Issued | 30 | 07/05/2005 | FABRICATION OF STRAINED SEMICONDUCTOR-ON-INSULATOR (SSOI) STRUCTURES BY USING STRAINED INSULATING LAYERS | IEONG, MEIKEI |

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| 11162780 | Not Issued | 30 | 09/22/2005 | HIGHLY MANUFACTURABLE SRAM CELLS IN SUBSTRATES WITH HYBRID CRYSTAL ORIENTATION | IEONG, MEIKEI |
| 11164215 | Not Issued | 20 | 11/15/2005 | QUASI SELF-ALIGNED SOURCE/DRAIN FinFET PROCESS | IEONG, MEIKEI |
| 11183062 | Not Issued | 30 | 07/15/2005 | Buried stress isolation for high-performance CMOS technology | IEONG, MEIKEI |
| 11207216 | Not Issued | 30 | 08/19/2005 | Dual trench isolation for CMOS with hybrid orientations | IEONG, MEIKEI |
| 11327966 | Not Issued | 25 | 01/09/2006 | CMOS on hybrid substrate with different crystal orientations using silicon-to-silicon direct wafer bonding | IEONG, MEIKEI |
| 60534916 | Not Issued | 159 | 01/07/2004 | Enhancement of electron and hole mobilities in <110> Si under biaxial compressive strain | IEONG, MEIKEI |

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|--------------------------|-------------------------|--------|------------|---|------------------------|
| 11162478 | Not Issued | 30 | 09/12/2005 | ANTI-HALO COMPENSATION | OLDIGES, PHILIP |
| 09525726 | Not Issued | 161 | 03/14/2000 | Semiconductor device having short-channel immunity | OLDIGES, PHILIP J. |
| 10604907 | 6924517 | 150 | 08/26/2003 | THIN CHANNEL FET WITH RECESSED SOURCE/DRAINS AND EXTENSIONS | OLDIGES, PHILIP J. |
| 10708378 | Not Issued | 41 | 02/27/2004 | HYBRID SOI/BULK SEMICONDUCTOR TRANSISTORS | OLDIGES, PHILIP J. |
| 10710277 | Not Issued | 71 | 06/30/2004 | STRUCTURE AND METHOD FOR MANUFACTURING PLANAR SOI SUBSTRATE WITH MULTIPLE ORIENTATIONS | OLDIGES, PHILIP J. |
| 10711182 | Not Issued | 19 | 01/01/0001 | Structure and method of making double-gated self-aligned finfet having gates of different lengths | OLDIGES, PHILIP J. |
| 10904483 | Not Issued | 93 | 11/12/2004 | HEATER FOR ANNEALING TRAPPED CHARGE IN A SEMICONDUCTOR DEVICE | OLDIGES, PHILIP J. |
| 10905906 | Not Issued | 30 | 01/26/2005 | CAPACITOR BELOW THE BURIED OXIDE OF SOI CMOS TECHNOLOGIES FOR PROTECTION AGAINST SOFT ERRORS | OLDIGES, PHILIP J. |
| 10905978 | Not Issued | 30 | 01/28/2005 | STRUCTURE AND METHOD FOR MANUFACTURING PLANAR STRAINED Si/SiGe SUBSTRATE WITH MULTIPLE ORIENTATIONS AND DIFFERENT STRESS LEVELS | OLDIGES, PHILIP J. |
| 11095373 | Not Issued | 30 | 03/31/2005 | MOSFET structure with ultra-low K spacer | OLDIGES, PHILIP J. |
| 09778335 | 6686630 | 150 | 02/07/2001 | DAMASCENE DOUBLE-GATE MOSFET STRUCTURE AND ITS FABRICATION METHOD | OLDIGES, PHILIP JOSEPH |

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First Name = MIN

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|--------------------------|------------|--------|------------|--|-----------------|
| 07342098 | Not Issued | 161 | 04/21/1989 | NOVEL LUMINOUS INFLATION TOY, ORNAMENT AND MARKING | YANG CHAO, MING |
| 60062112 | Not Issued | 159 | 10/14/1997 | RESIN COMPOSITION HAVING IMPROVED CHEMICAL AND /OR WATER RESISTANCE | YANG ZHAO, MING |
| 08067834 | 5445993 | 150 | 05/27/1993 | SEMICONDUCTOR LASER DIODE AND METHOD FOR MANUFACTURING THE SAME | YANG, MIN |
| 09784963 | 6451702 | 150 | 02/16/2001 | METHODS FOR FORMING LATERAL TRENCH OPTICAL DETECTORS | YANG, MIN |
| 10033902 | 6667528 | 150 | 01/03/2002 | SEMICONDUCTOR-ON-INSULATOR LATERAL P-I-N PHOTODETECTOR WITH A REFLECTING MIRROR AND BACKSIDE CONTACT AND METHOD FOR FORMING THE SAME | YANG, MIN |
| 10250241 | Not Issued | 61 | 06/17/2003 | High-performance CMOS devices on hybrid crystal oriented substrates | YANG, MIN |
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